UTILITY APPLICATION FOR UNITED STATES PATENT

FOR

SEMICONDUCTOR MEMORY DEVICE HAVING TAG BLOCK FOR REDUCING
INITIALIZATION TIME

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SEMICONDUCTOR MEMORY DEVICE

HAVING TAG BLOCK FOR REDUCING INITIALIZATION TIME

Field of Invention

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The present invention relates to a semiconductor memory device; and, more particularly, to a tag block, for use in the semiconductor memory device, for reducing an initialization time at data access.

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Description of Prior Art

Generally, a semiconductor memory device is classified as a random access memory (RAM) and a read only memory (ROM).

15   The RAM includes a Dynamic RAM (DRAM) and a Static RAM (SRAM). One cell of the dynamic RAM has one transistor and one capacitor and that of the static RAM does four transistors and two load resistances. The DRAM is used more widespread than the SRAM because the DRAM is more efficient than SRAM in

20   a chip integration and a manufacturing process.

Today, an operation speed of a central processing unit (CPU) is more dramatically advanced than that of the DRAM. As a result, many problems may arise because the operation speed of the memory device is slower than that of CPU. For

25   overcoming these problems, several kinds of scheme in the memory device have been developed for a high speed data transmission.

1

Fig. 1 is a block diagram showing a bank in a conventional semiconductor memory device disclosed in a commonly owned copending application, U.S. Ser. No._____, filed on Oct. 29, 2003, entitled "SEMICONDUCTOR MEMORY DEVICE

5   WITH REDUCED DATA ACCESS TIME", which is incorporated herein by reference.

As shown, the bank includes a cell area 10, a tag block 30, a predetermined cell block table 20 and a control block 40. The cell area 10 has N+1 number of unit cell blocks and a data

10 latch block 70. Also, in each unit cell block, M number of word lines is coupled to a plurality of unit cells. The N and M are positive integers. Herein, N is 8 and M is 256. In addition, a size of memory device, i.e., a storage capability, is calculated with the exception of the additional unit cell

15 block. Namely, a size of the bank is M(number of word lines) × N(number of unit cell blocks) × (number of bit lines). The predetermined cell block table 20 includes a plurality of registers for storing predetermined restore cell block address information. The predetermined restore cell block address

20 information contains at least one predetermined restore cell block address among (8+1)×256 word line addresses. The tag block 30 generates a target restore cell block address corresponding to an access cell block address based on the predetermined restore cell block address information. The

25 control block 40 controls the predetermined cell block table 20, the cell area 10 and the tag block 30 in order to support an cell block interleaving mode which can make the memory

2

device operate on high speed without reduction of data access time when at least two data accesses are sequentially occurred in the same bank.

Herein, the cell block interleaving mode is defined as an operation that, during a current data in response to a current instruction is restored in the original cell block or in another cell block, a next data in response to a next instruction is simultaneously outputted from the same cell block.

In addition, a row address inputted to the control block 40 of the memory device corresponds to 8×256 word lines; and the other word lines, i.e., 256 word lines of additional cell block are assigned as predetermined word lines. However, the predetermined word lines are not fixed but changed during an operation of the memory device.

Fig. 2 is a block diagram depicting the tag block 30 shown in Fig. 1.

As shown, the tag block 30 includes the 8+1 number of unit tag tables 110A to 110I, the 8+1 number of comparators 100A to 100I, a cell block address decoder 32, a cell block address encoder 34 and a tag control unit 38.

The cell block address decoder 32 receives a available restore cell block address Extra_BA outputted from the predetermined cell block table 20 and selects one among unit tag tables 110A to 110I in response to the available restore cell block address Extra_BA. Then, the comparator, e.g., 100A compares an address of converting a current row address Cur_RA

based on the selected unit tag table with a logical cell block address Cur_LBA. And last, the cell block address encoder 1834 outputs a current restore physical cell block address Cur_PBA which is encoded in response to a result of comparison.

Herein, each of the unit tag tables 110A to 110I stores a restore cell block address information corresponding to N×256 word lines of unit cell blocks.

The tag block 30 further includes a delay unit 36 for delaying the current restore physical cell block Cur_PBA by one clock period to access a restore cell block.

Herein, each of unit tag tables 110A to 110I has 256 registers, and one register LBA consists of three bits because the number of the logical cell block addresses is 8. For instance, the first unit tag table 110A stores information what logical cell block is corresponded with each 256 numbers of the word lines included in the first unit cell block, and the second unit tag table 110B stores information what logical cell block is corresponded with each of 256 numbers of the word lines included in the second unit cell block.

In addition, in each unit tag table 110A to 110I, the first register 0 stores the logical cell block address in response to the word line 'WL0' of each unit cell block, the second register 1 stores the logical cell block address in response to the word line 'WL1' of each unit cell block, and 256th register 255 stores the logical cell block address in response to the word line 'WL255' of each unit cell block.

For example, referring to the first unit tag table 110A,

4

first register 0 stores '1' and 255th register 255 stores '7'. That is, in the first unit cell block, first word line WL0 corresponds with first word line WL0 of the second logical unit cell block and 255th word line WL255 corresponds with 255th word line WL255 of the eighth logical unit cell block.

Fig. 3 a block diagram describing the predetermined cell block table 20 shown in Fig. 1.

As shown, the predetermined cell block table 20 includes 256 registers, each having the predetermined restore cell block address information. The predetermined restore cell block address information contains a predetermined restore cell block address. The predetermined restore cell block address consists of 4 bits because the number of physical unit cell blocks is nine. The predetermined restore cell block address information represents a target cell block to be restored, corresponding to an accessed word line of unit cell block.

For instance, referring to the predetermined restore cell block address stored in each register, a first register 0 stores '1' and a second register 1 stores '3'. That is, a predetermined word line of a first word line WL0 is a first word line WL0 of the second unit cell block and a predetermined word line of a second word line WL1 is a second word line WL0 of the forth unit cell block. Herein, during the operation of the memory device, 256 registers of the predetermined cell block table are continuously updated.

The predetermined cell block table 20 receives a current

5

row address Cur_RA, a previous row address Pre_RA and a previous restore physical cell block address Pre_PBA. Also, the predetermined cell block table 20 is updated by an updating signal EBT_UP DATE. The predetermined cell block
5   table 20 outputs an available restore cell block address Extra_BA to the tag block 30.

Fig. 4 is a block diagram showing the unit tag table, e.g., 110A shown in Fig. 2.

As shown, the unit tag table 110A is enabled by a
10   decoded signal dec-Extra_BA outputted from the cell block address decoder 32 and receives the logical cell block address Cur_LBA and the local address Cur_RA. The local address Cur_RA is a kind of address for selecting one among 256 number of word lines included in one unit cell block.

15   The unit tag table 110A includes 256 register which can store 3-bit data. Data stored in a register selected by the local address Cur_RA is outputted as a selected logical cell block address LBA_OUT. Also, at updating a register, the register selected by the local address Cur_RA is updated into
20   the logical cell block address Cur_LBA.

Fig. 5 is a timing diagram describing operation of the memory device shown in Fig. 1; and, especially, describes the intra cell block interleaving mode when a first and a second data are sequentially accessed in the same unit cell block
25   among 8+1 numbers of the unit cell blocks shown in Fig. 1.

Hereinafter, referring to Figs. 1 to 5, there is described the operation of the conventional memory device

6

shown in Fig. 1.

The additional unit cell block is used for restoring the first data when the second data are sequentially accessed in the same unit cell block. As shown in Fig. 5, the first data is stored in unit cells coupled to a first word line WL0, and the second data is stored in unit cells coupled to a second word line WL1 of the same unit cell block.

First, at a first timing period t0, the first word line WL0 of, e.g., first unit cell block is activated in response to a first instruction CD0; and, then, first data in response to the first word line WL0 is sensed and amplified. The amplified first data moves to the data latch block 70.

If the first instruction CD0 is a read instruction, data in response to the first instruction CD0 among K number of data latched in the data latch block 70 is outputted; otherwise, i.e., if the first instruction CD0 is a write instruction, data in response to the first instruction CD0 among K number of data latched in the data latch block 70 is overwritten by an inputted data of external circuit.

At a second timing period t1, first, the second word line WL1 of, e.g., first unit cell block is activated in response to a second instruction CD1; and, at the same time, the first word line WL0 of, e.g., third unit cell block is activated.

Then, the second data in response to the second word line WL1 is sensed and amplified; and, at the same time, the first data is restored into unit cells in response to the first word line WL0 of the third unit cell block.

As described above, the data access time of the conventional memory device can be actually precluded the data restoration time, because the second data can be sensed and amplified by the next instruction during the first data in response to the present instruction is restored. Thus, the data access time can be effectively reduced to thereby obtain a high speed operation of the memory device. In addition, in the conventional memory device, the data restoration operation can be simplified by simply changing only the cell block address of the data.

In the other hand, hereinafter, there is described the inter cell block interleaving mode when a third and a forth data are sequentially accessed in each different unit cell block among 8+1 numbers of the unit cell blocks (not shown).

Contrary to the intra cell block interleaving mode, the third data outputted from a unit cell block is stored in the original unit cell block at the same timing of outputting the forth data from another unit cell block.

In this case, the data access time of the conventional memory device can be actually precluded the data restoration time, because the forth data can be sensed and amplified by the next instruction during the third data in response to the present instruction is restored.

In the conventional memory device, the inputted cell block address is considered as the logical unit cell block address, i.e., address for selecting one among 8 unit cell blocks. But the conventional memory device actually includes

8

8+1 unit cell blocks, so the inputted cell block address is converted into a physical unit cell block address. This process is carried out by the control block 40.

Herein, each unit tag table included in the tag block 30 of the conventional memory device shown in Fig. 1 should be initialized at an initialization operation. As shown in Fig. 2, each unit tag table should be selected in order for being initialized. Then, the local address Cur_RA is inputted; and the logical cell block address storing initial value is inputted. For instance, the local address Cur_RA is inputted in order from '0' to '255' and the logical cell block address is inputted as '0'. After initializing the first unit tag table 110A, the second unit tag table 110B is initialized by the same manner.

Therefore, for initializing all unit tag table, the initialization operation is performed 256×9 times. For operating the memory device in high speed, the initialization operation of the unit tag block should be simplified and carried out during short time.

Summary of Invention

It is, therefore, an object of the present invention to provide a method and an apparatus of a memory device for accessing data on high speed so that the data restoration time does not affect seriously the data access time.

In accordance with an aspect of the present invention,

9

there is provided a semiconductor memory device including a cell area having N+1 number of unit cell blocks, each including M number of word lines; a predetermined cell block table for storing a candidate information representing at

5   least more than one candidate word line among the M number of the word lines to be stored data; and a tag block for receiving a row address, sensing a logical cell block address in the row address and outputting a physical cell block address based on the logical cell block address and the

10   candidate information, wherein the tag block includes: a N+1 number of unit tag tables, each having M number of registers and storing a store information that the registers corresponds to M number of word lines, each register storing each the physical unit cell block address in response to the logical

15   cell block among unit cell block addresses having a word line in response to the candidate information; and an initialization unit for initializing the N+1 number of unit tag tables.

In accordance with another aspect of the present

20   invention, there is provided a method for controlling a tag block for assigning a physical unit cell address based on a logical unit cell block, including the steps of: a) initializing the tag block in a semiconductor memory device; and b) performing a normal operation of the semiconductor

25   memory device by using the tag block.

Brief Description of Drawings

The above and other objects and features of the present invention will become apparent from the following description of preferred embodiments taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a segment in a conventional semiconductor memory device;

Fig. 2 is an exemplary block diagram depicting a tag block shown in Fig. 1;

Fig. 3 is an exemplary block diagram describing a predetermined cell block table shown in Fig. 1;

Fig. 4 is a block diagram showing a block diagram showing a unit tag table shown in Fig. 2;

Fig. 5 is a timing diagram describing the operation of the memory device described in Fig. 1;

Fig. 6 is a block diagram showing a segment in a semiconductor memory device in accordance with the present invention; and

Fig. 7 is a detailed block diagram depicting an initialization unit shown in Fig. 6.

Detailed Description of the Invention

Hereinafter, a semiconductor memory device having an advanced data strobe circuit according to the present invention will be described in detail referring to the

11

accompanying drawings.

Fig. 6 is a block diagram showing a bank in a semiconductor memory device in accordance with the present invention.

5   As shown, the bank includes a cell area 600, a predetermined cell block table 620, a tag block 630 and a control unit 640. The cell area 600 has 8+1 number of unit cell blocks, each including 256 number of word lines for responding to an inputted row address. A row address is

10   inputted in response to eight unit cell blocks. Herein, the cell area 600 further includes additional unit cell block. The predetermined cell block table 620 is used for storing information wherein at least more than one word line among the (8+1)×256 number of the word lines is assigned as a

15   predetermined restorable word line by using the information. The tag block 630 receives the row address, senses a logical cell block address designated for accessing one of N number of unit cell blocks, converts the logical cell block address into a physical cell block address designated for accessing one of

20   the N+1 number of unit cell blocks and outputs the physical cell block address. The control unit 640 is used for controlling the tag block 630 and the predetermined cell block table 620 for activating one word line of a unit cell block selected by the physical cell block address.

25   Herein, the tag block 630 includes an N+1 number of unit tag tables 632A to 632I for storing information that 256 number of word lines included in each of 8+1 number of unit

12

cell blocks correspond to the logical unit cell block; and an initialization unit 634 for initializing the 8+1 number of unit tag tables.

Fig. 7 is a detailed block diagram depicting an initialization unit shown in Fig. 6.

As shown, the initialization unit 634 includes a plurality of logical OR gates 635A to 635I, a plurality of first multiplexers 636A to 636I and a plurality of second multiplexers 637A to 637I.

The plurality of logical OR gates 635A to 635I are used for respectively receiving an initialization selection signal IE to nullify all of the 8+1 number of unit tag tables and each of tag table selection signals dec-Ectra_BA0 to dec-Ectra_BA8 to select one of the 8+1 number of unit tag tables and respectively outputting each of initialization activating signals to each of the N+1 number of unit tag tables.

The plurality of first multiplexers 636A to 636I are controlled by the initialization selection signal IE for selectively outputting one between the input logical cell block address Cur_LBA and each of initialization signals BN0 to BN8 to initialize each of the N+1 number of unit tag tables to each of the N+1 number of unit tag tables.

The plurality of second multiplexers 637A to 637I are controlled by the initialization selection signal IE for selectively outputting one between a local address Cur_RA to select M number of word lines included in each of the N+1 number of unit cell blocks and an initialization address

13

All_RA to select all register included in one of the unit tag table.

Hereinafter, referring to Figs. 6 and 7, an initializing operation of the semiconductor memory device in accordance with the present invention is described in detail.

If an initialization operation is started, nine(8+1) unit tag tables 632A to 632I included in the tag block 630 are simultaneously selected by inputting the initialization activating signals outputted from nine(8+1) logical OR gates after the initialization selection signal IE is inputted to the nine(8+1) logical OR gates. Also, the plurality of first multiplexers 636A to 636I respectively output each of the initialization signals BN0 to BN8 to each of the nine unit tag tables 632A to 632I.

After the initialization operation, in the nine unit tag tables 632A to 632I, eight unit tag tables store first to eighth logical cell block addresses and the extra one is a predetermined cell block for restoring data.

At the initialization operation, eight unit tag tables among the nine unit tag tables 632A to 632I respectively store each different logical cell block address. For instance, the first unit tag table 632A stores the first logical cell block address and the second unit tag table 632B stores the second logical cell block address.

In detail, the unit tag table has 256 number of registers, each having 3 bits, because the 256 registers included in the unit tag table respectively stores information

14

that each of 256 word lines of the unit cell block corresponds to which logical cell block. Namely, at the initialization operation, 256 registers of the first unit tag table 632A individually store '0' which means the first logical unit cell block; and 256 registers of the second unit tag table 632B individually store '1' which means the second logical unit cell block.

For storing each initialized logical cell block address in 256 registers of the unit tag table, each of the plurality of second multiplexers 637A to 637I outputs the initialization address All_RA to each of unit tag tables 632A to 632I. If the unit tag table receives the initialization address All_RA, 256 registers store inputted initialization signal, e.g., BN0.

Thus, after the initialization operation, the first to the eighth unit tag tables 632A to 632H respectively have 256 registers, each storing '0' to '7'. And, 256 registers of the ninth unit tag table 632I do not have to store any particular initialization value, e.g, '0' or '1', because the 256 registers of ninth unit tag tables correspond to the predetermined cell block.

Therefore, the present invention can dramatically reduces initializing time for initializing the tag block by performing the initialization operation on all unit tag tables of the tag block at once.

In addition, an operation speed of the semiconductor memory device having the tag block in accordance with the present invention is advanced by reducing the initializing

15

time for initializing the tag block.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modification 5 may be made without departing from the spirit and scope of the invention as defined in the following claims.